REMARKS

In the Office Action, Claims 1-24 are pending and were examined. Claims 1-10 are allowed and Claims 11-24 are rejected. In this Response, Claims 11-13, 16, 18 and 20-23 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending claims in view of the following remarks.

I. Claims Rejection under 35 U.S.C. §112

The Examiner has rejected Claims 11, 16 and 21 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 11, 16 and 21 are rejected for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed had possession of the claimed inventions.

Regarding Claims 11 and 21, Claims 11 and 21 are amended as follows to overcome the 35 U.S.C. §112, first paragraph rejection:

> instructing the completion queue whether or not to discard a completion packet received from a designated end-device if the completion queue is loaded with header information from one of the modified, non-posted request cycle and the generated, new request cycle. (Emphasis added.)

As correctly noted by the Examiner, the discarding of the completion packet, as recited by Claims 11 and 21, is applicable to either the modified, non-posted request cycle or the generated new request cycle. Accordingly, Applicants have amended Claims 11 and 21 such that the instructing of whether or not to disregard a completion packet received from a designated end user device is limited to completion packets received for either modified non-posted request cycles or the generated, new request cycles.

Accordingly, in view of Applicants' amendment to Claims 11 and 21, Applicants respectfully submit that Claims 11 and 21, as amended, now contain subject matter which is subscribed in the specification in such way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, has possession of the claimed

invention. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph rejection of Claims 11 and 21.

Claim 16 is further rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Regarding Claim 16, Claim 16 is amended to recite the following claims feather to overcome the 35 U.S.C. §112, second paragraph rejection:

> wherein the control logic instructs the completion queue whether or not to return a completion packet if the completion queue is loaded with header information from one of the modified non-posted request cycle and the generated, the new request cycle to the requesting device. (Emphasis added.)

Applicants respectfully submit that the above amendment to Claim 16 limits the instruction of whether to return a completion packet to modified non-posted request cycles as well as the generated request, new request cycles, and hence, it is not applicable to the captured non-posted request cycle, as indicated by the Examiner.

Accordingly, in view of Applicants' amendment to Claim 16, Applicants respectfully submit that Claim 16, as amended, now particularly points out distinctly the claimed subject matter which the Applicants regard as an invention. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph rejection of Claim 16.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 11-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,158,018 to Bernasconi et al. ("Bernasconi") in view of U.S. Patent No. 5,966,547 to Hagan et al. ("Hagan"). Applicants respectfully traverse this rejection.

Regarding Claims 11 and 21, Claims 11 and 21 are amended to recite the following claim feature, which is neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan:

> instructing the completion queue whether or not to discard a completion packet received from a designated end-device if the completion queue is loaded with header information from one of the modified, non-posted request cycle and the generated, new request cycle. (Emphasis added.)

Applicant respectfully submits that the above-recited feature of amended Claims 11 and 21 is analogous to the features of allowed Claim 1. Hence, Applicants respectfully submit that the prior art combination of Bernasconi in view of Hagan fails to provide any teachings or suggestions regarding instructing a completion queue whether or not to discard a completion packet received from a designated end-device if the completion queue is loaded with header information from one of the modified, non-posted request cycle and the generated, new request cycle, as recited by amended Claims 11 and 21.

Furthermore, Applicants respectfully submit that the Examiner's interpretation of the term "incoming request cycle" is unreasonable. According to the Examiner:

> Bernasconi discloses a method comprising: "receiving an incoming request cycle (24) from a requesting device (16); determining if the received incoming request cycle matches one or more of preprogrammed trigger conditions (col. 9, lines 51-57, teaches that the trigger-matching logic is the logic that doest the matching between the current DSP program address and a break address correspond to a flawed DSP program stored in the ROM 18, such as at section 18b). (pg. 5, ¶1 of the Office Action mailed August 30, 2006.)

As indicated by the cited passage above, the Examiner asserts that FIG. 1 of Bernasconi discloses the determination of whether an incoming request cycle matches a programmed trigger condition, as recited by amended Claims 11 and 21. Applicants respectfully disagree with the Examiner. As taught by Bernasconi:

> Again with respect to FIG. 1, a bus 24 provides the current DSP program address from the embedded DSP 16 (hereafter more simply referred to as "DS") to the patching circuitry 22, the ROM 18, and the RAM 20. Additionally, DSP program software stored in the ROM 18 is provided via bus 26, the patching circuitry 22, and bus 30 to the DSP 16. Similarly, corrected DSP program software stored in the ROM 18 is provided via bus 26, the patching circuitry 22, and bus 30 to the DSP 16. Similarly, corrected DSP program software stored in the RAM 20 such as section 20b of the RAM 20 is provided via bus 28, the patching circuitry 22, and bus 30 to the DSP 16. (col. 6, lines 15-23.) (Emphasis added.)

As indicated by the cited passage above, reference numeral "24" of FIG. 1 refers to a bus, which as taught by Bernasconi, provides the current DSP program address from the embedded DSP 16 to the patching circuitry 22, the ROM 18 and the RAM 20. (*See*, supra.) As further disclosed by Bernasconi, the DSP program address is compared against a break address to identify flawed DSP program software embedded within ROM 18. (*See*, col. 9, lines 53-57.)

Applicant respectfully submits that MPEP §2111.01 requires that THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAN MEANING;" to wit, the MPEP has established that "PLAN MEANING" REFERS TO THE ORDINARY AND CUSTOMARY MEANING GIVEN TO THE TERM BY THOSE OF ORDINARY SKILL IN THE ART.

Regarding the term "request cycles," Applicant's specification describes two categories of such request cycles, including a write request cycle that is used to transport data from a host processor to an end-user device or a read request cycle that is used to read data from the end-user device. (*See*, pg. 1, ¶3 of Applicant's specification.) In addition, Applicant has defined the term "non-posted request cycles" to include any request cycle that requires completion including, but not limited to, memory requests, configuration read requests and configuration write requests. (*See*, pg. 4, ¶0016, lines 10-14 of Applicant's specification.)

Applicant respectfully submits that the meaning of the term "incoming request cycle" to a person of ordinary skill in the art of interconnect design at the time of the invention would not include the receipt of current DSP program address over bus 24 from DSP 16 to patching circuitry 22, ROM 18 and RAM 20 to identify flawed DSP program software embedded in ROM 18, as taught by Bernasconi. Hence, the Examiner's interpretation of the term "incoming request cycle" to include the receipt of a current DSP program address received from bus 24 is unduly broad and unreasonable since the interpretation disregards the "plain meaning" of the term to one of ordinary skill in the art of interconnect design at the time of the invention, such as the PCI Express Interconnect Protocol (see Applicants' Specification, pp. 5, ¶ 00016.)

As mandated by case law, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

As correctly noted by the Examiner:

> Bernasconi fails to specifically teach specifying whether the I/O controller including a patch module (patching circuitry 22) coupled to a completion queue is to be loaded with information from non-posted cycle. (pg. 3, ¶3 of the Office Action mailed April 21, 2006.)

As a result, the Examiner cites Hagan. Hagan is directed to a method and process for posting events or tasks to a shared queue and a multi-processor data processing system to post events or tasks to another processor to perform. (*See*, col. 1, lines 10-17.) Applicant respectfully submits that the communication between such processors to post events or tasks to another processor to perform provides no teaching or suggestion regarding the non-posted request cycles, as referred to by amended Claims 11 and 21. Furthermore, Hagan fails to rectify the failure of Bernasconi to provide any teaching or suggestion regarding instructing a completion queue whether or not to discard a completion packet received from a designated end-device if the completion queue is loaded with header information from one of the modified, non-posted request cycle and the generated, new request cycle, as recited by amended Claims 11 and 21.

Hence, Applicant respectfully submits that the Examiner is prohibited from establishing a *prima facie* case of obviousness of amended Claims 11 and 21, since all limitations recited by amended Claims 11 and 21 are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan. Id.

Consequently, Applicant respectfully submits that Claims 11 and 21, as amended, are patentable over the combination of Bernasconi in view of Hagan, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claims 11 and 21.

Regarding Claims 12-15 and 22-24, Claims 12-15 and 22-24, based on their dependency from Claims 11 and 21, respectively, are also patentable over the prior art combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 12-15 and 22-24.

Regarding Claim 16, Claim 16, as amended, recites the following claim features, which are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan:

> a control logic coupled to the trigger-matching logic to select a set of instructions upon detection of at least one matched trigger condition and to execute operations as specified by the selected set of instructions, wherein if the captured request cycle that caused a trigger is a non-posted request cycle, the control logic instructs a completion queue to load the completion queue with one of the following (1) unmodified header information from the captured non-posted request cycle, (2) modified header information associated with modified non-posted request cycle, or (3) header information associated with a new request cycle generated in response the captured request cycle,
>
> wherein the control logic instructs the completion queue whether or not to return a completion packet if the completion queue is loaded with header information from one of the modified non-posted request cycle and the generated, the new request cycle to the requesting device. (Emphasis added.)

As indicated by the above-recited features of amended Claim 16, the above-recited feature of amended Claim 16 recites an analogous claim feature to amended Claims 11 and 21:

> wherein the control logic instructs the completion queue whether or not to return a completion packet if the completion queue is loaded with header information from one of the modified non-posted request cycle and the generated, the new request cycle to the requesting device. (Emphasis added.)

Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of amended Claims 11 and 21, as unpatentable over the prior art combination of Bernasconi in view of Hagan, equally apply to the §103(a) rejection of Claim 16 as unpatentable over such references. Hence, for at least the reasons provided above, Applicant respectfully submits that Applicant's amendment to Claim 16 prohibits the Examiner from establishing a *prima facie* case of obviousness of amended Claim 16, since all claim limitations recited by amended Claim 16 are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan. Id.

Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 16, as amended, is patentable over the prior combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 16.

Regarding Claims 17, 18 and 20, Claims 17, 18 and 20, based on their dependency from Claim 16, are also patentable over the prior art combination of Bernasconi in view of Hagan. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 17, 18 and 20, as amended, are patentable over the prior combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17, 18 and 20.

III. Allowable Subject Matter

The Examiner has indicated that Claims 1-10 are allowable because the prior art of record fails to disclose "instructing the completion queue whether or not to discard a completion packet received from a designated end-devices." Applicants respectfully thank the Examiner for recognizing the allowability of Claims 1-10.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: October 30 , 2006

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF FASCIMILLE TRANSMISSION:
I hereby certify that this correspondence is being transmitted via facsimile on the date below, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Annie McNally 10/30/2006
Annie McNally